DBBC3 Development

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1 INAF-IRA, 2 MPIfR, 3 OSO

The Project

- Supported by EU Radionet3
- DIVA – Task2
- Partner:

    INAF – Italy

    MPIfR - Germany

    OSO – Sweden

DBBC3 Project is oriented to:

Astronomy

- **EVN wide-band VLBI backend**
- **EHT (Event Horizon Telescope)**

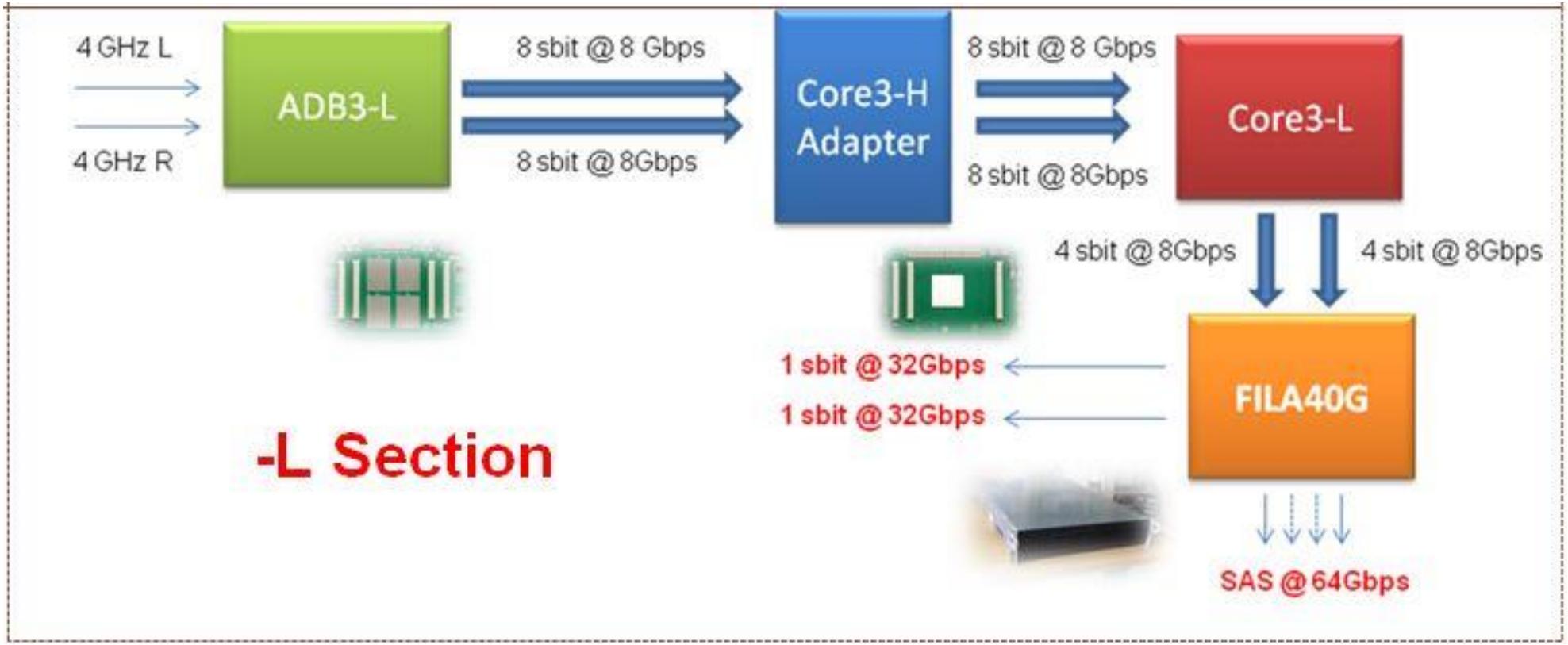
Geodesy

- **VGOS ultra-wide-band VLBI system**

EVN - EHT – VGOS with DBBC3-L
General Performance

- Number of RF/IF in one system: **std. 2 (8 for VGOS)**
- Instantaneous bandwidth ea. sampler: **4 GHz**
- Sampling representation: **10 bit**
- Processing capability**: std. 24** (**max 96) TMACS** (multiplication-accumulation/s)
- Output: **VDIF 10GE/40GE packets, 32/64/128 Gbps**
- Observing Modes: **DDC/PFB/WB-DDC/WB-PFB/SDC**
- Compatibility with existing DBBC environment

DBBC3-L Architecture for EVN and EHT



CURRENT STATUS

GCoMo (GigaConditioningModule)

Additional element to adapt the receivers

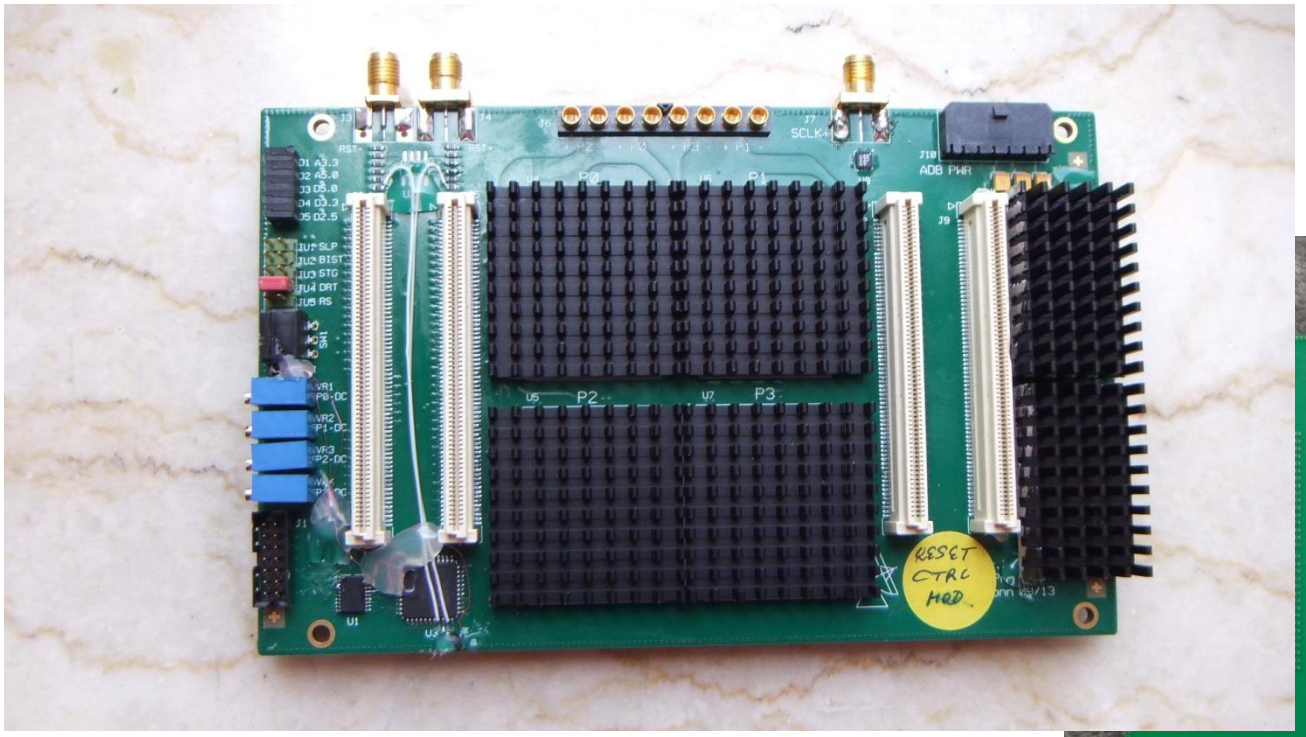
- Downconvert pre-filtered pieces of 4 GHz bwd
- Input range: up to 16 GHz
- Number of channels: 2 pre-filtered 4 GHz bands
- Total power detectors: 2 independent
- Modular construction
- Power level control in agc and manual mode
- Compatibility with existing DBBC environment
- Status: **First Prototypes available**

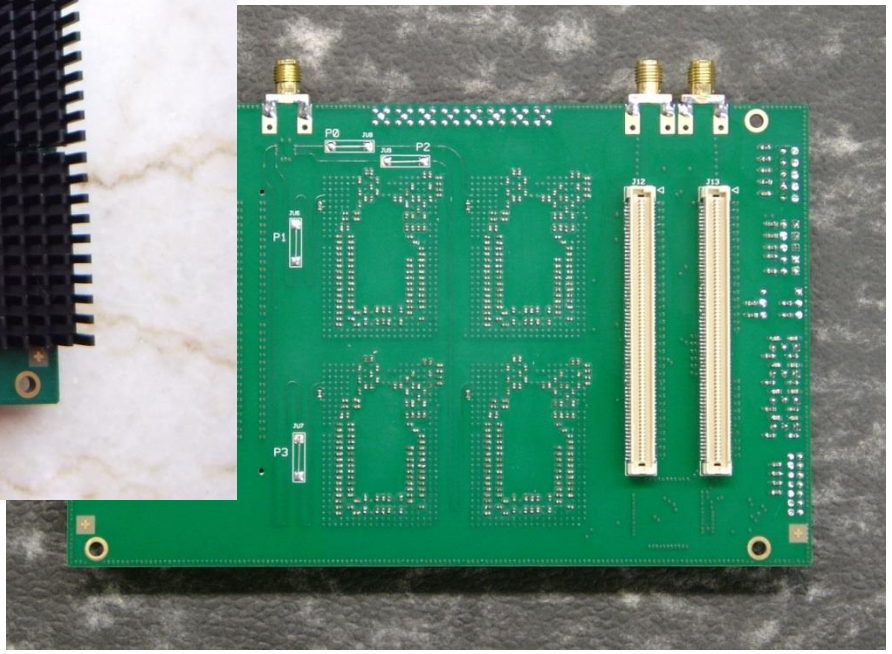
ADB3L - Sampler board

- Number of IFs: **1 - 4**
- Equivalent Sample Rate: **2-4-8 GSps**
- Instantaneous bandwidth: **4-2-1 GHz**
- Sampling representation: **10 bit**
- Real/Complex Sampling
- Compatibility with existing DBBC environment

Status ADB3L

Prototype ready debugged, final revision under construction



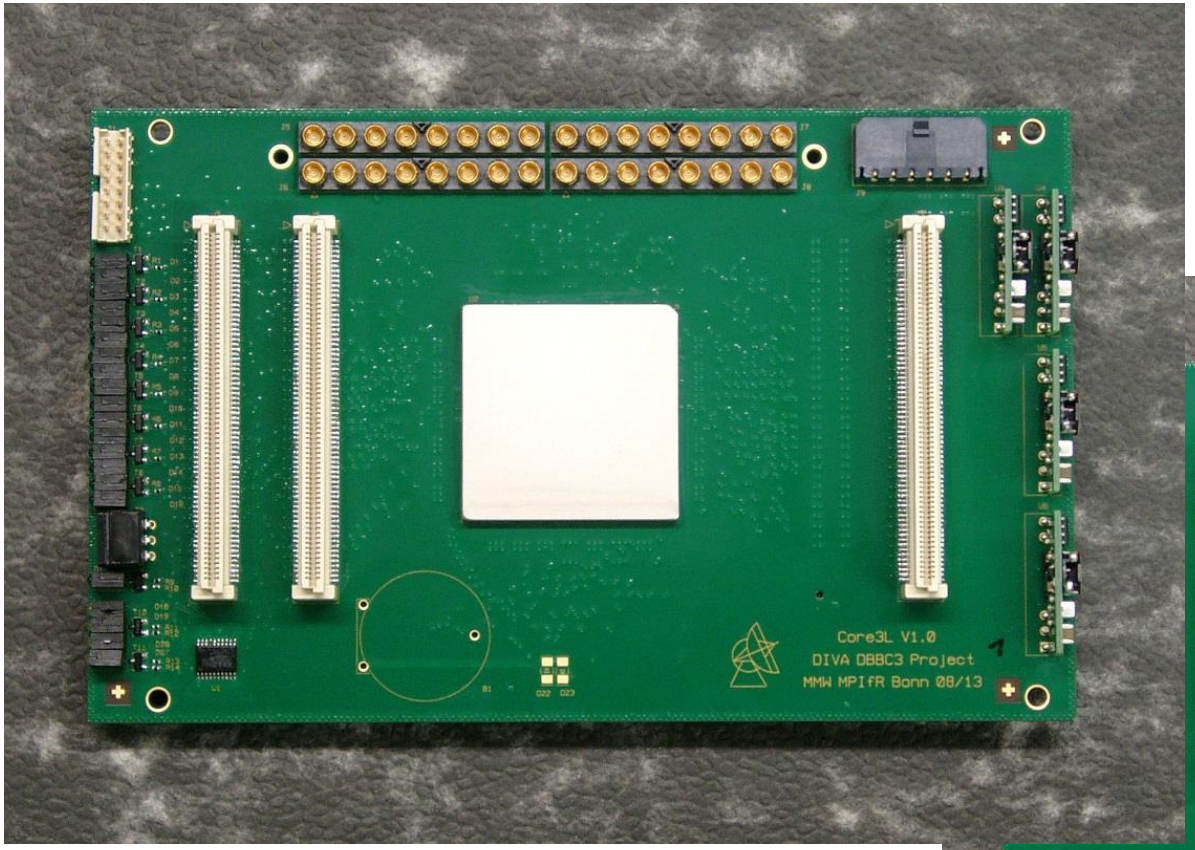


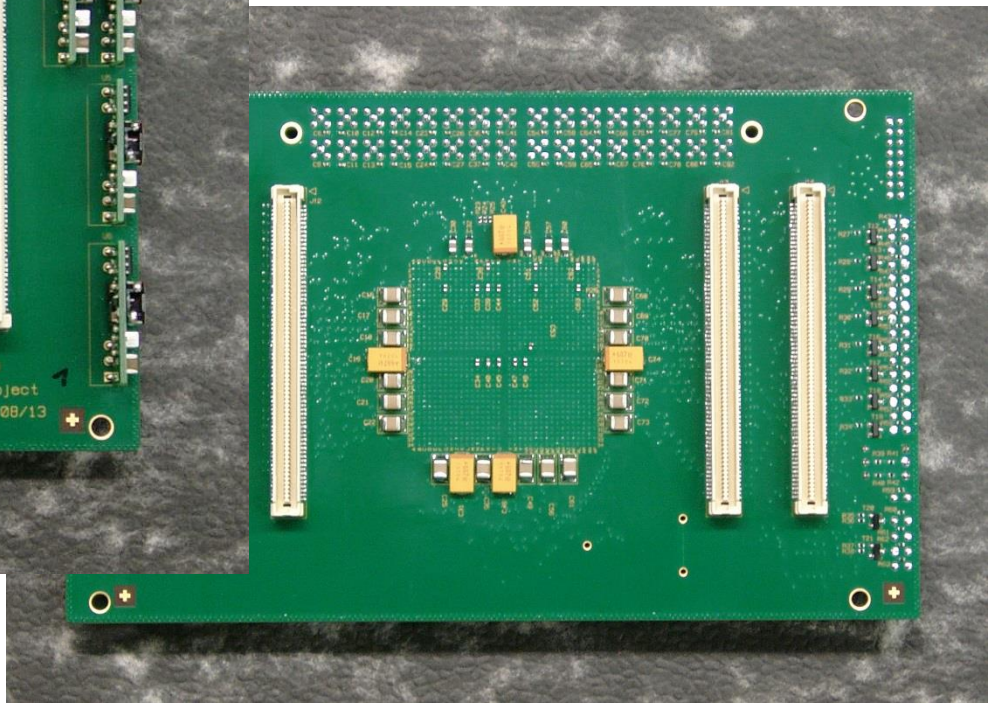
CORE3L - Processing board

- Number of I/O: **max 40 serial links 12.5Gbps**
- Number of Output: **max 32 serial links 11.2Gbps**
- Input Sampling Representation: **8-10 bit**
- Processing capability: **max 3 TMACS** (multiplication-accumulation per second)
- Processing capability: **DDC, PFB, WB-DDC, WB-PFB, DCS**
- Output: **VDIF 10GE packets**
- Compatibility with existing DBBC environment

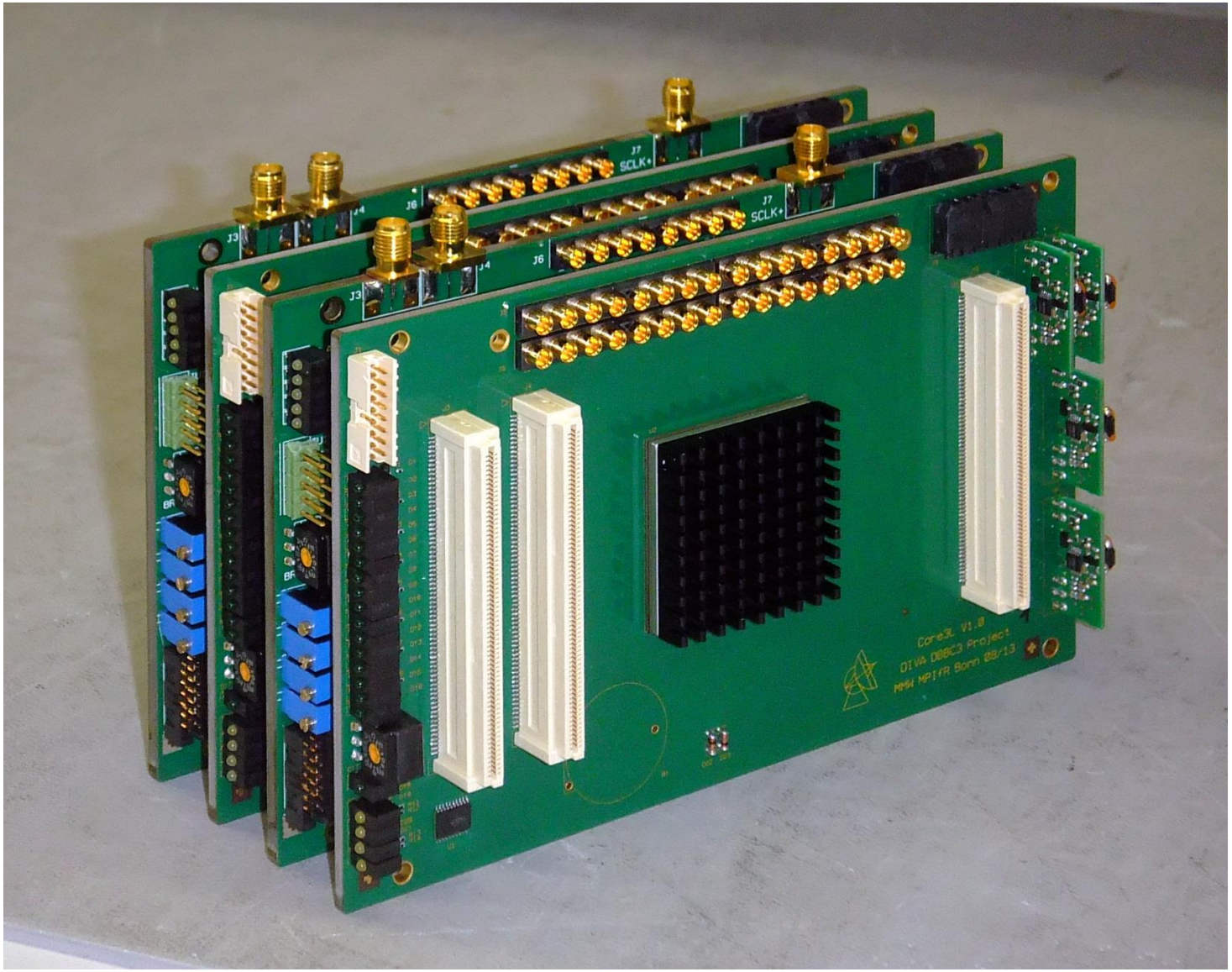
Status CORE3L

Prototype debugged, final version under construction





EVN/EHT: Stack with 2 ADB3L and 2 CORE3L
4 GHz bwd real dual polarization



D B B C 3
EUROPEAN
NETWORK
HAT Lab

CORE3L: Firmware aboard

- DDC existing modes available in the DBBC2 (implemented)
- PFB existing modes available in the DBBC2 (implemented)
- SDC existing full band 0.5 – 1 GHz (implemented)

- WB-DDC tunable 128-64-32-16-8 MHz U&L (under way)
- WB-PFB fixed continuous 256 MHz (under way)
- SDC full band 2 – 4 GHz (under way)

CORE3L: 10GE Communication skills available aboard

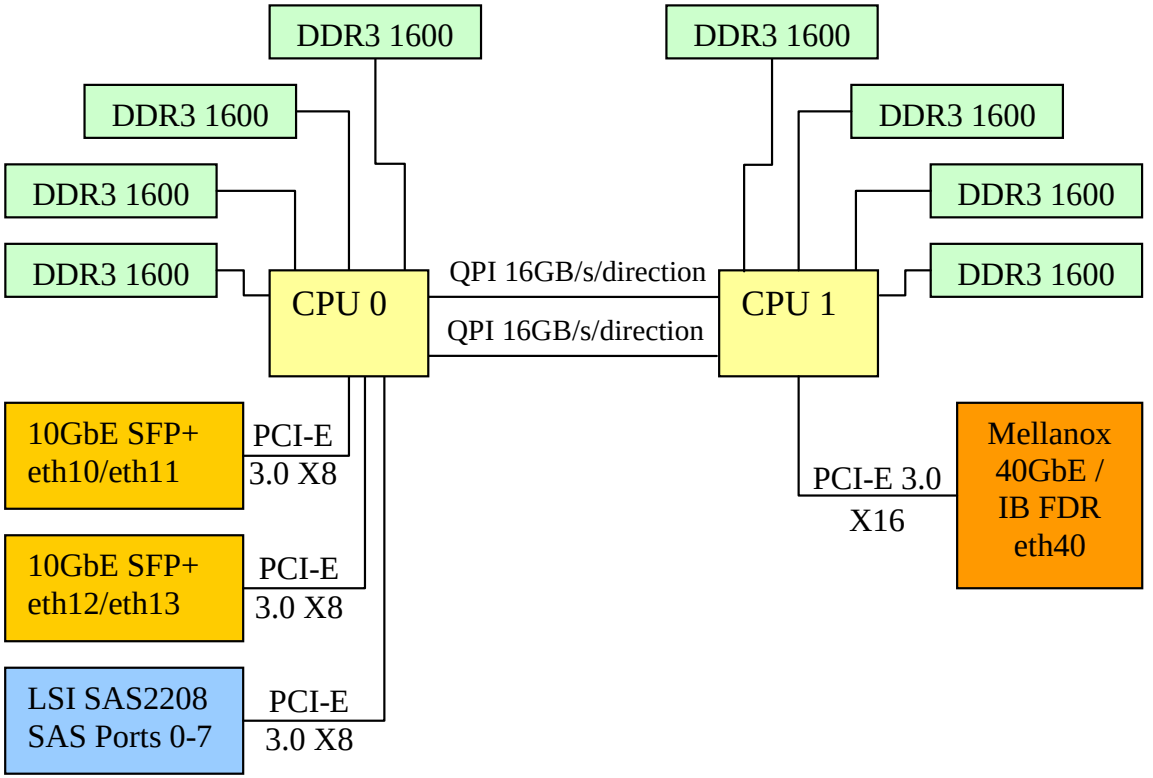
- MK5B up to 4 Gbps (native is 2Gbps)
- VDIF Single Thread up to 8Gbps/10G port
- VDIF Multiple Threads up to 8Gbps/10G port
- RAW (no headers) up to 8Gbps/10G port
- Threads can be fed by a selection of data channels eventually corner-turned
- The 10G Ethernet ports are independent in the destination address in VDIF-ST and MK5B
- The 10G Ethernet ports in multi-thread mode support an independent block of destination addresses coupled with the thread content selection
- Decimation and bit-mask selectable

FILA40G General Key features

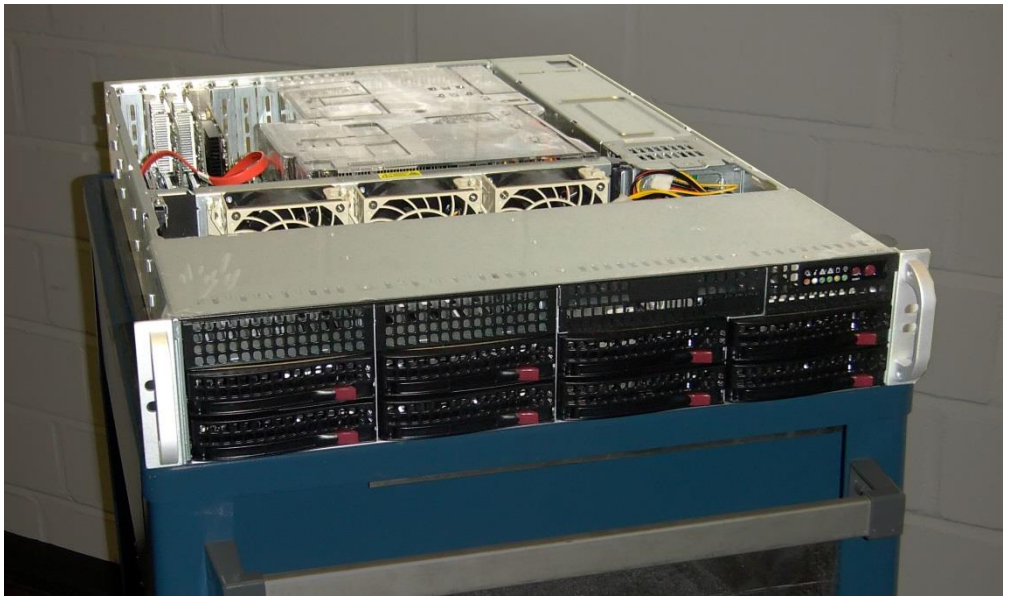
- 8 x 10GE Inputs
- 2 x 40GE Output
- Optional disk storage
  - Expected to record at 32Gbps sustained in half configuration mode
  - Compatibilty with Mark6 disk packs/chassis being investigated
- Stream aggregation
- Format conversion/VDIF threading
- Packet filtering
- Pulsar gating
- Timekeeping via NTP and/or GPS module
  - Propagates UTC to other connected devices via DBBC Local Network (DLN)

FILA40G Architecture for 32 Gbps

- 2 x Intel Xeon E5-2670
  - 8 core 2.60 GHz
- 8 x 8GB DDR3 1600
- 8 Onboard SAS2 ports
- 4 free PCI 3.0 x8 slots
  - To be used to add extra SAS2/3 ports



Status FILA40G 3 systems assembled + 40G Protocol Analyzer available (MPI)



TEST AND OBSERVATIONS

- **Zero baseline planned before the end of 2014 in Bonn with 2 and 4 GHz bandwidth**

- **On-field VLBI test at 4 GHz bwd planned in the first months of 2015 between Noto-Effelsberg-Onsala at 22 GHz**

THANKS! QUESTIONS?