Minutes from the meeting of: Thursday June 14 2012
Present: Jonathan, Salvatore, Des, Harro

Action items of last meeting

Harro: Kristine made a Wiki account for Jonathan and Jonathan uploaded three
documents: the design document, a how-to document describing testing with Erlang and the UniBoard and a how-to about the start-up sequence of the correlator. Sergei's document still needs to be uploaded

Harro: a simple short test using tcpdump on the uni-ctl computer was done and it was shown that all the expected packets (four backnodes sending 1024 packets each, so 4096 packets in total) arrive at the uni-ctl machine. Erlang seems to be the problem where they get dropped. Des and Harro will investigate.

Individual updates

All: all of us had another in-depth meeting with Sergei in the afternoon of Thursday June 7th on "the model". Sergei explained the finer bits of how to apply the model in a correlator and specifically in the UniBoard correlator.
It was again very insightfull. Des intends to make a documet out of it once finished digesting it.

Jonathan/Salvatore: the hardcoded delay coefficients were removed from the design. Reception of the coefficients, using the UDP offload port in Eric's ethernet module, in the VHDL has been confirmed. There
is still a small issue with the FIFO but that turned out to be a question of
using the right clock (gated in stead of not gated).

Furthermore Jonathan and Salvatore have been busy testing with sending sine waves through the correlator. The way the tests were performed was by sending the same sine to both stations. By playing around with the delay coefficients (0 samples, few samples and ~1/2 period) the phase of the signal, at the correlation peak, changes. The phase shift was predicted using the MATLAB model and the observed phase shift matched the model to better than 1%.

There may or may not be an issue with the imaginary part in the autocorrelation. It is not exactly 0 (as it should be) but there is signal to the level of about 1000:1 (30dB). It is unknown at this moment if this is
a bug or a feature and if feature: is it good enough? Salvatore mentions it may be a feature of the PFB design which was borrowed from LOFAR.

Another suggestion was to integrate a noisy sine wave for a prolonged time and see if something systematic shows up. We'll see what Jonathan and Salvatore will end up doing.

The issue regarding treating validity bits was not discussed yet. Des

promised he'd discuss with SFXC people to find out how they treat validity bits so we know where we can/should cut corners.

Daniel v/d Schuur has made modifications to the uniboard compilation scripts
and the sopc design to include the memory map "system.h" into the NiosII memory. This allows any client program to read out which components are present in the firmware. For generic UniBoard software this would be a good thing to have (in the Erlang code) but for the EVN correlator is was deemed not really necessary.

Action items

Jonathan: upload Sergei's two page document about mixer and FFT.

Des/Harro: investigate Erlang performance problems reading UDP packets

Salvatore: find someone in LOFAR who knows the details of the PFB,
check if they know about the behaviour and why they think it is acceptable.
May need discussing with Sergei and/or SFXC people depending on outcome.

Des: figure out validity bit handling in SFXC

pro memori:

Jonathan/Salvatore: update output data packet header with 8-bit FPGA node-id
and possible >1 bit correlation engine id. Update documentation and put on the memoseries wiki.

all: write up documentation and upload to wiki

Next meeting

The date of the next meeting is June 21st, immediately after JIVE coffee.