Correlator Implementation and Control meeting

Thursday, April 15 2010, 15.00, Minnaert room

Present: Sergei, Jonathan, Ying, Eric, Harro, Des, Arpad

Agenda

- test firmware, status and timeline
- correlator firmware
- correlator control code and NIOS OS
- aob

Jonathan: explained (de)packetizer that he is designing with SOPC builder, using a XAUI interface, configuration via NIOS, FIFO to fabric. Can be tested with a PC generating UDP packets. Problem with hard and soft-core XAUI blocks (only 3 hard-core, but adding 1 soft-core does not work, all 4 should be soft-core, which takes way too much logic). This problem was supposed to have been solved in new version of Quartus.

Memory modules have been ordered, so a model of these actual modules can now be used in the design.

Discussion started on whether VDIF packets should contain one or two pols. Harro and Des were working under the assumption that these should be independent. Sergei pointed out that combining two pols, both 4 bits, into one byte would be by far the most hardware-efficient solution. Decision was made to stick to this for the first version of the correlator at least.

Eric told about modular design approach which he is trying to define, which would make re-use and combining of pieces of firmware much easier through uniform interfaces. Would be very useful for the project, especially if more groups start participating. Document is on the way, will be discussed internally first, then with other project partners.

Harro has run the NIOS C-code on a PC, with an erlang control system sending commands. He is now waiting for an ethernet interface to the test FPGA boards, which Eric is working on. Des continues work on VEX parser and database structure.