

JUC, 12-01-2018, 11.00

present Harro, Des, Jonathan, Benito, Arpad

Jonathan: unhappy state of UB after last e could not be analysed. Looks like DDR controller got jammed. Will un-outcomment signal tap. 16 and 32 MHz versions should have same fixes.

However, 1000B packets has not been tested with 32MHz. Possibly possible to use 2000B packets, but who knows if Fila will work ok then. Jonathan will check, signal taps should also be inserted in 32MHz version. May not be possible for next week though. Des should fix model for e.

Next week e-run: use 32 MHz version first, during test time. Then continue after e next day, have both 32 and 16 versions ready. New images on both UBs.

Benito: will do one of his current expts soon, both SFXC and JUC.