Correlator control and implementation meeting, August 2, 2012, Minnaert

Present: Jonathan, Jintao, Harro, Aard, Paul, Arpad

Short discussion about action items, all remain not done.

Main focus of meeting: discuss design consideration doc that Arpad wrote and sent around, and email of Harro outlining a way to synchronise correlator, data and coefficient sources.

Unfortunately Arpad let a bit too much time pass by, and did not take many notes, as it was a fairly free-flowing discussion. The minutes of this meeting will consequently be rather sketchy.

By and large those present agreed with the conclusions of the design doc. Harro suggested I might want to add some info on data output rates. The doc, with slight modifications, has been sent around since then to the MT members (for whom it was meant in the first place). Should also be placed in the memo series.
***action Arpad

Harro then explained his scheme, using the white board. Basically, there will be a small buffer, a FIFO, in the FPGA that says full or empty. The correlator reads data from memory for processing and when the amount of data falls below a certain threshold sets the buffer condition to empty. The control computer polls the buffer, and as soon as it reads empty sends one second worth of data to the UB, and resets it to full. In this way, the correlator speed should only be limited by the slowest data sender (and the speed of the correlator itself of course), and the problem of missing data can be very easily solved. If there is no data, the data sender must have the intelligence to reply that it has sent the data. The correlator correlates on, marking whatever data it reads from DDR as invalid. Some tuning will be necessary of course, and a sufficiently smart data sender has to be implemented (should probably be separate from jive5ab).

This will of course also have to be documented properly, but that will have to wait until Harro returns from vacation.