BRAND STATUS UPDATE

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On behalf of the BRAND team:

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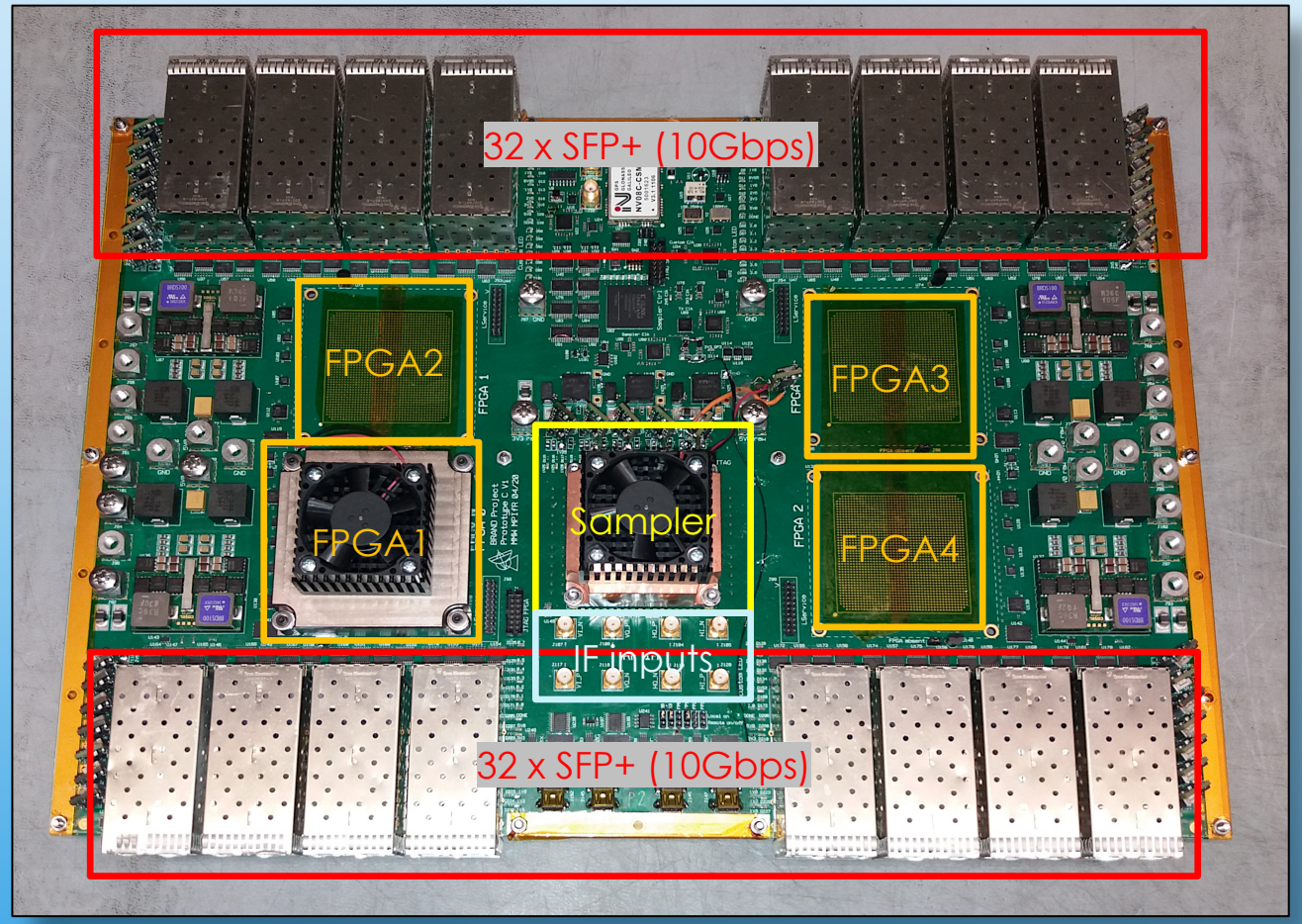
BRAND PROJECT

- BRAND was part of EC-funded Joint Research Activity (JRA)
- Formally ended end of 2020
- Goal: build broad band receiver prototype for Effelsberg
  - 1.5 -15.5 GHz
  - Direct sampling; no down-conversion

- Status:
  - Finished: analogue components, feed, digital backend
  - Finished: digital frontend
  - Pending: integration and testing of Effelsberg prototype

BRAND DIGITAL FRONTEND



BRAND_C (PCB 3rd revision)
- 30x40 cm
- 22 layers

IF Inputs (2 options):
- 2 x 28 GHz
- 4 x 14 GHz

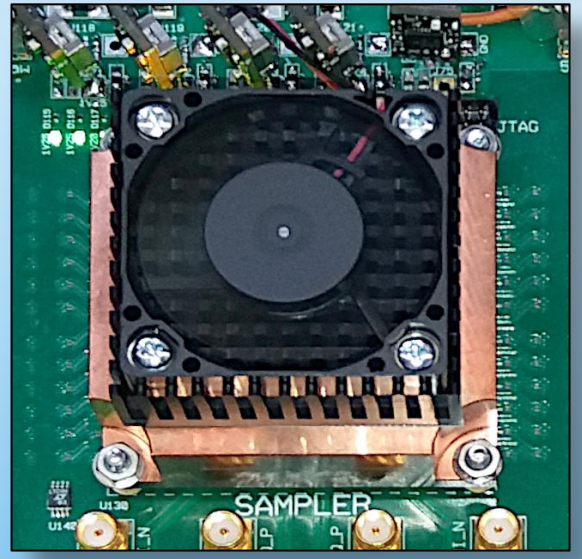
Outputs:
- 64 x 10 Gbit

FPGAs:
- 4 x Xilinx Kintex Ultrascale

Sampler:
- 2x 57.6 Gsps @8bit

Power supply
- Max. 100A @ 0.95V (FPGA)

BRAND DIGITAL FRONTEND - SAMPLER



Sampler:

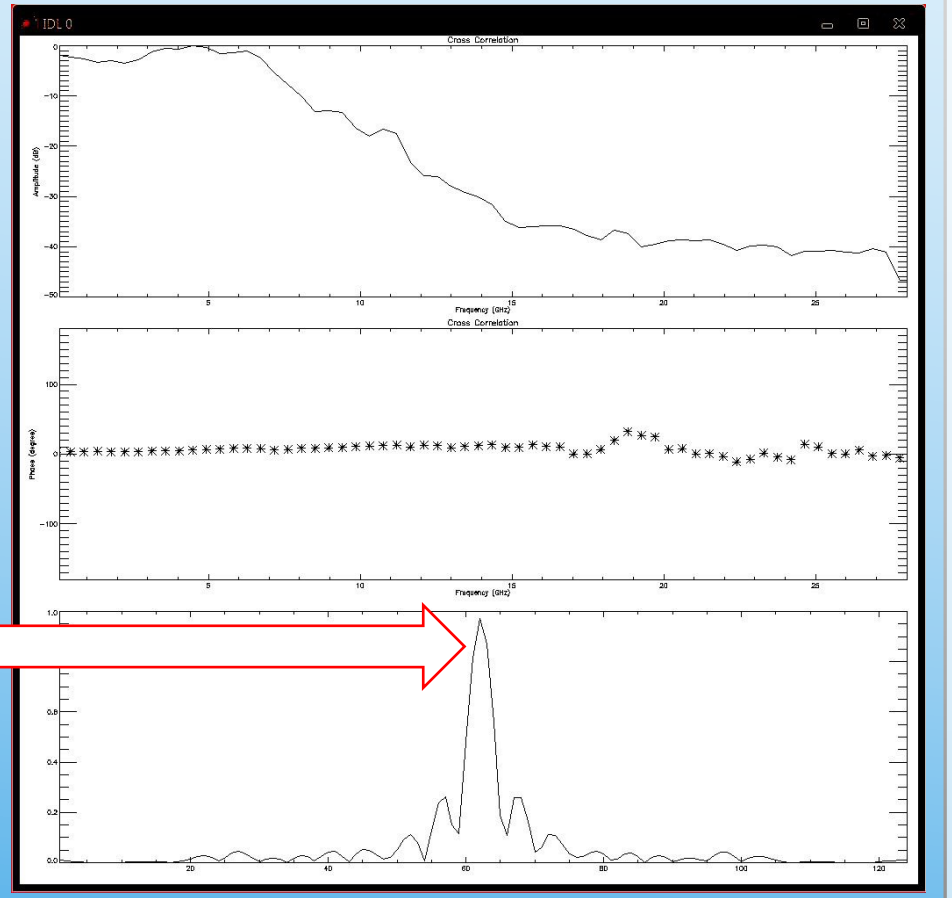
Total sample rate 115.2 Gsps @8bit on a single chip (2 options)

- 2 x 57.6 Gsps
- 4 x 28.8 Gsps

Effective bits: 6.5

Output: via 96 high-speed parallel lanes

Assembly of the the 96 output lines into a valid, fully-sampled data stream by 4 on-board FPGAs.



Zero-baseline fringe over the full band 0-28 GHz

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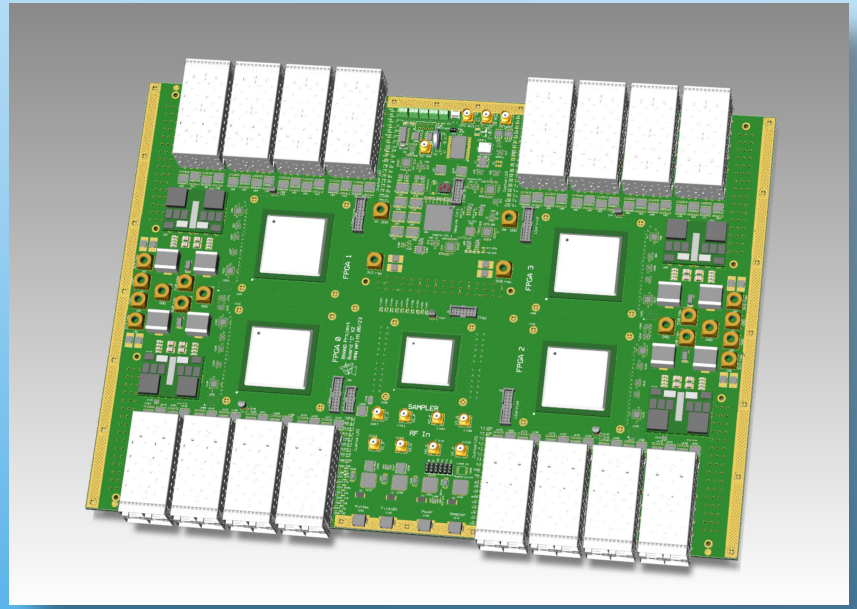
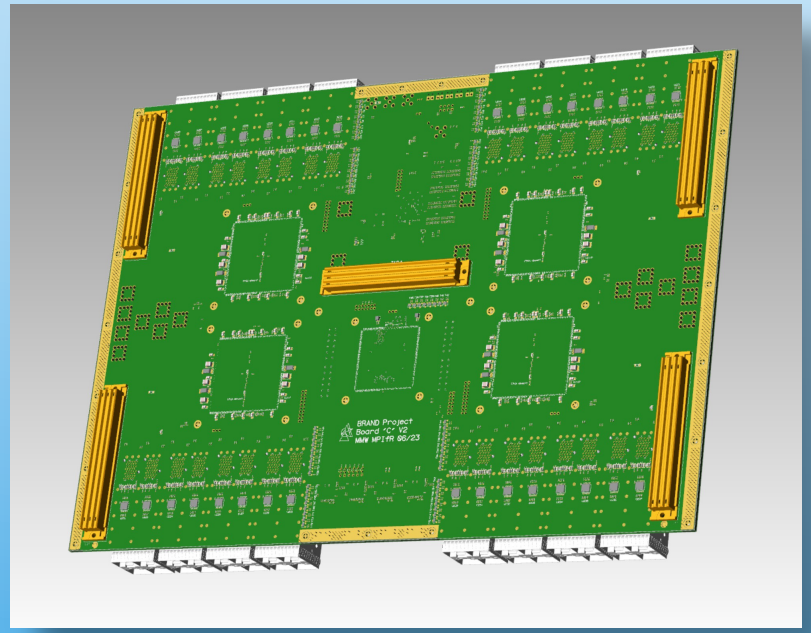
BRAND PCB VERSION2

Digital frontend “lessons learned”

=> design and production of BRAND PCB *Version 2*





Expected delivery of version2 boards

Spring 2024

BACKEND

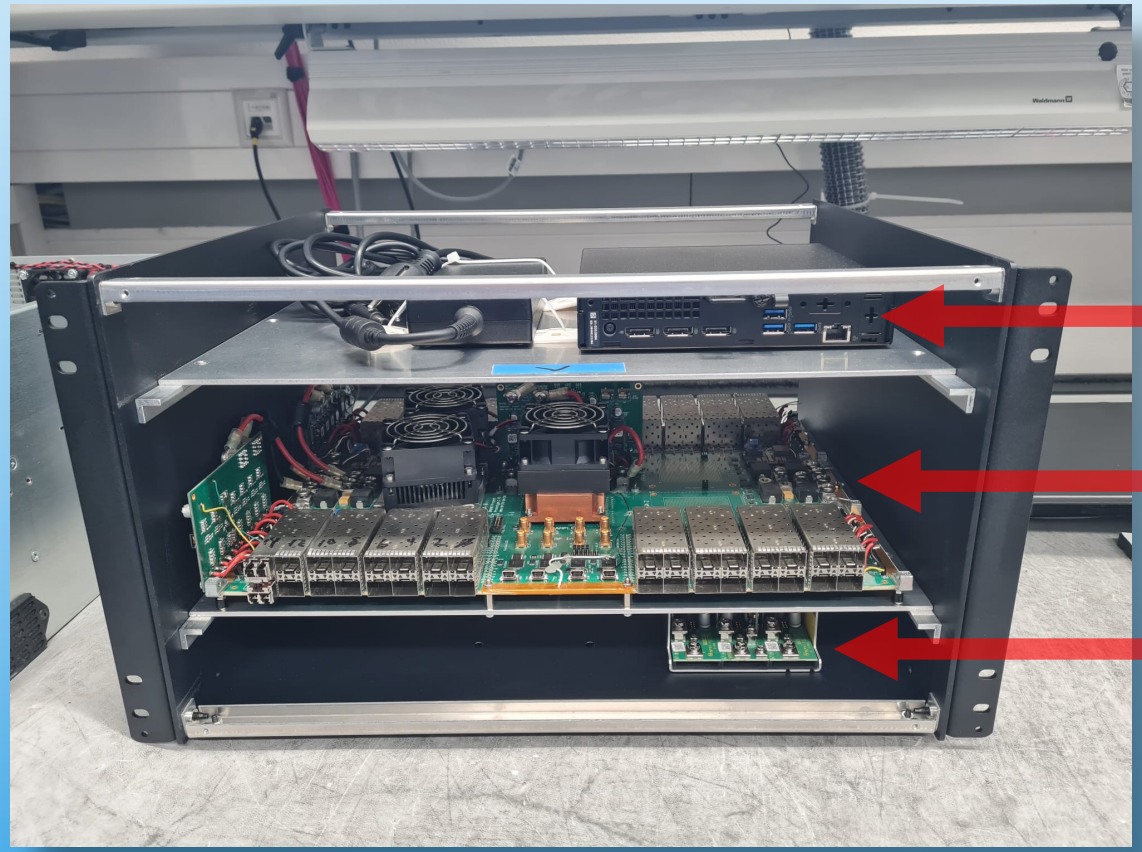
- Firmware “I”-mode successfully tested for the DBBC3 (see DDBC3 status presentation for details)

- DBBC3 will process digital input received by BRAND
  - Further sub-banding by DDC or OCT modes

FIRMWARE

- OCT_D
  - 2 filters per IF: 1.8, 3.6 GHz (in range 1.5 - 15.5 GHz)
  - Tested over the entre input band (zero-baseline, tone-injection)
- DDC
  - OCT block followed by 8 BBCs
  - Output bands: 112.5, 56.25, 28.125, 14.0625, ... 1.75... MHz LSB & USB
  - Currently under testing (zero-baseline, tone-injection)
  - Possible future modes
    - 1 x OCT filter followed by 16 BBCs
    - 2 x OCT filters followed by 4 BBCs
- DSC
  - 8-bit mode, OCT block?
  - Planned

DIGITAL FRONTEND INTEGRATION



Digital Frontend

- Control computer
- Digital frontend PCB
- Power supply

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SIGNAL TRANSPORT

RF-over-fibre

- Signal transport from prime focus to Faraday room
- 50 dB dynamic range

SYSTEM INTEGRATION

Integration and testing of the Effelsberg BRAND prototype

- Master thesis starting in January
- Duration 12 months
- Expected on-sky measurements in last quarter of 2024

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SAMPLER PROCUREMENT

MPIfR has procured **30** sampler chips (minimum order quantity)

- Sampler chips can be purchased by partners
  - BRAND receiver
  - DBBC4 backend
  - DiFrEnd28 sampling component