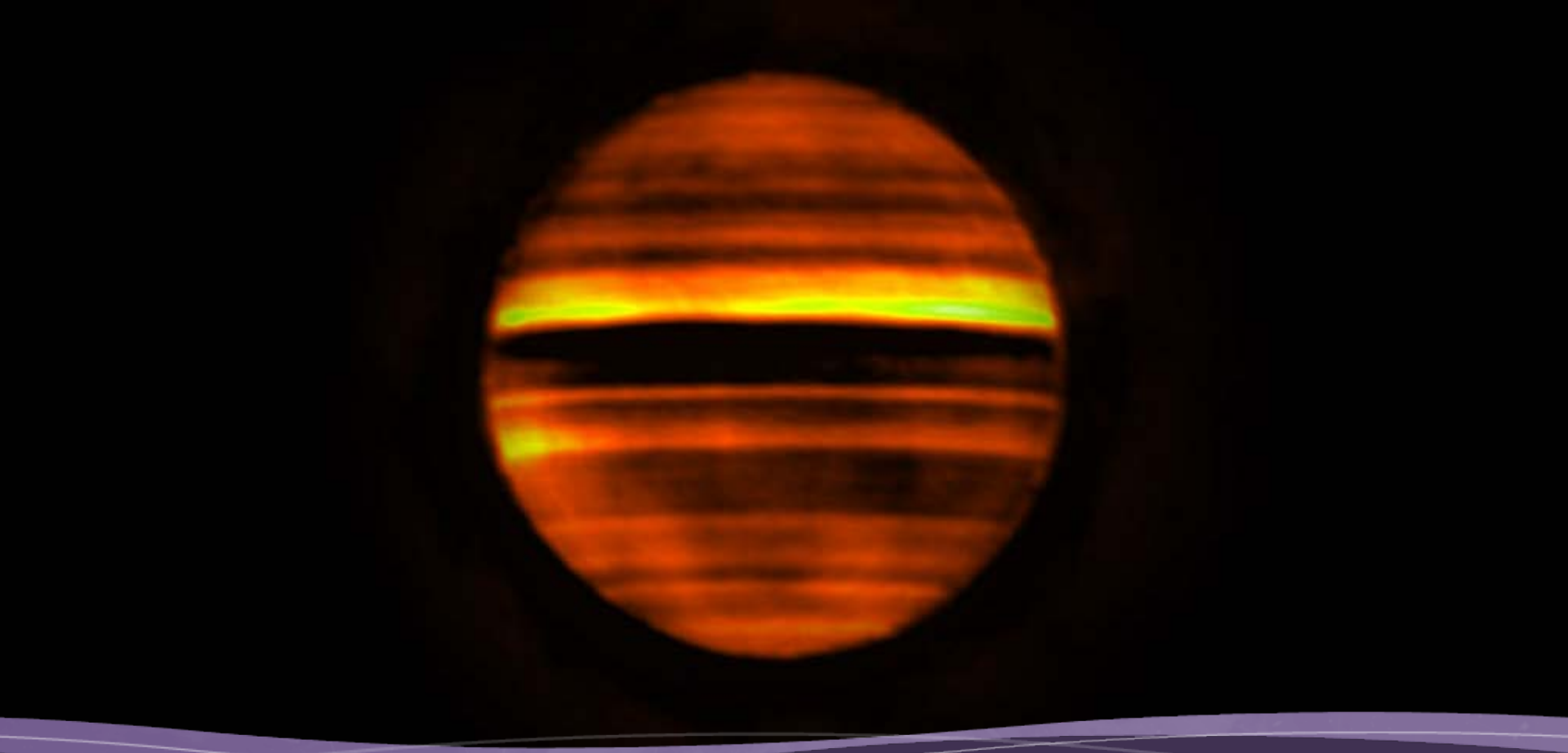


VLBA Status

Walter Brisken

Feb 03, 2021

VLBA: Status overview

- Infrastructure is aging, but generally functional
  - SC currently off line due to gearbox failure
  - Maser fleet refresh ongoing
- Several ongoing development activities:
  - VLBA New Digital Architecture
  - New flexibly frequency synthesizers
  - High speed networks to VLBA sites
  - Research grade GNSS receivers
  - New weather stations
- High Sensitivity Array (HSA)
  - Weakened due to Arecibo loss

COVID-19

- VLBA Ops has continued to operate, uninterrupted
- Back-up control room established
  - For use if main control room becomes contaminated
  - Tested one or two shifts per week
  - Put to actual use recently
- Major maintenance very limited
  - HN wheel/axel broke; carefully coordinated maint visit for repair
  - No other major maintenance (preventative or restorative) performed since Mar 2020
- Development projects generally are slowed

VLBA New Digital Architecture (VNDA)

- Project to replace the aging ROACH DBEs
  - Sample data
  - Channelize and quantize for VLBI processing
  - Time-tag and format
  - Demodulate "continuous cal" switched power

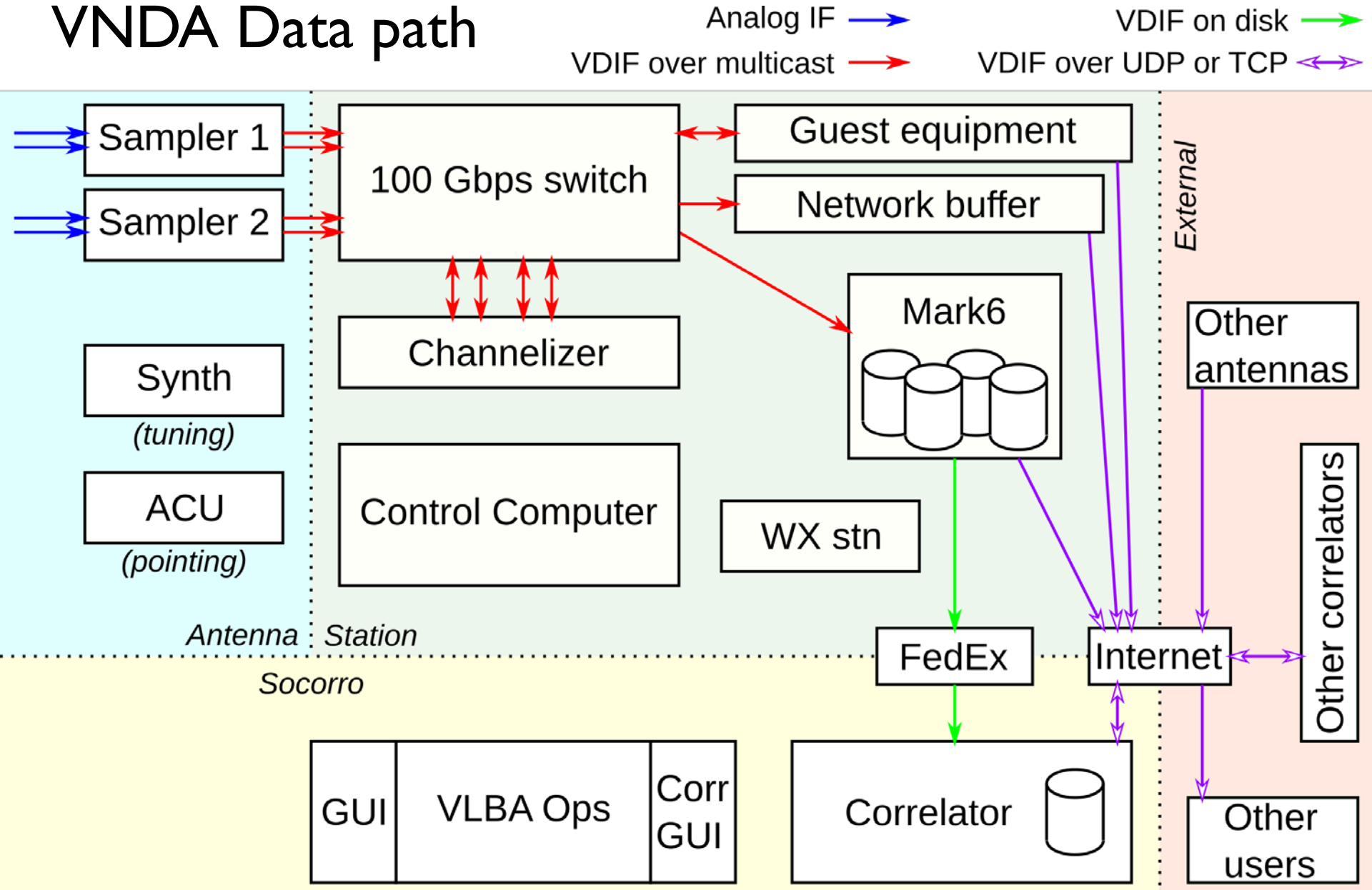
Requirements and design goals

- Backwards compatible with existing VLBA capabilities
- Provide gateway to higher bandwidths
- Support for 2, 4, or 8 (maybe 12) bits per sample
- Timing stability at sample level (no jumps)
- Support for non-VLBI use
  - E.g., pulsars, spectroscopy, transient searches
  - Some use cases may require user-supplied HW or SW
- Improve sustainability
  - Improved in RFI tolerance and avoidance
  - Improved compatibility with other VLBI systems
  - Reduced operations footprint
  - Increased maintainability

Engineering Approach

- Develop functional (superset) replacement of RDBEs
  - Stay focused on core functionality
  - Provide interfaces for future expansion
- Replacement system developed to following philosophies
  - Use commercial off-the-shelf (COTS) hardware where possible
  - Use standard interfaces and data formats where possible
  - Self diagnostic capabilities designed in from start
  - MTBF-informed design
  - Consider downstream obsolescence
  - Digitize as close to receivers as possible
  - Use multicast, to allow flexible re-use of signals

VNDA Data path



Make use of commercial equipment

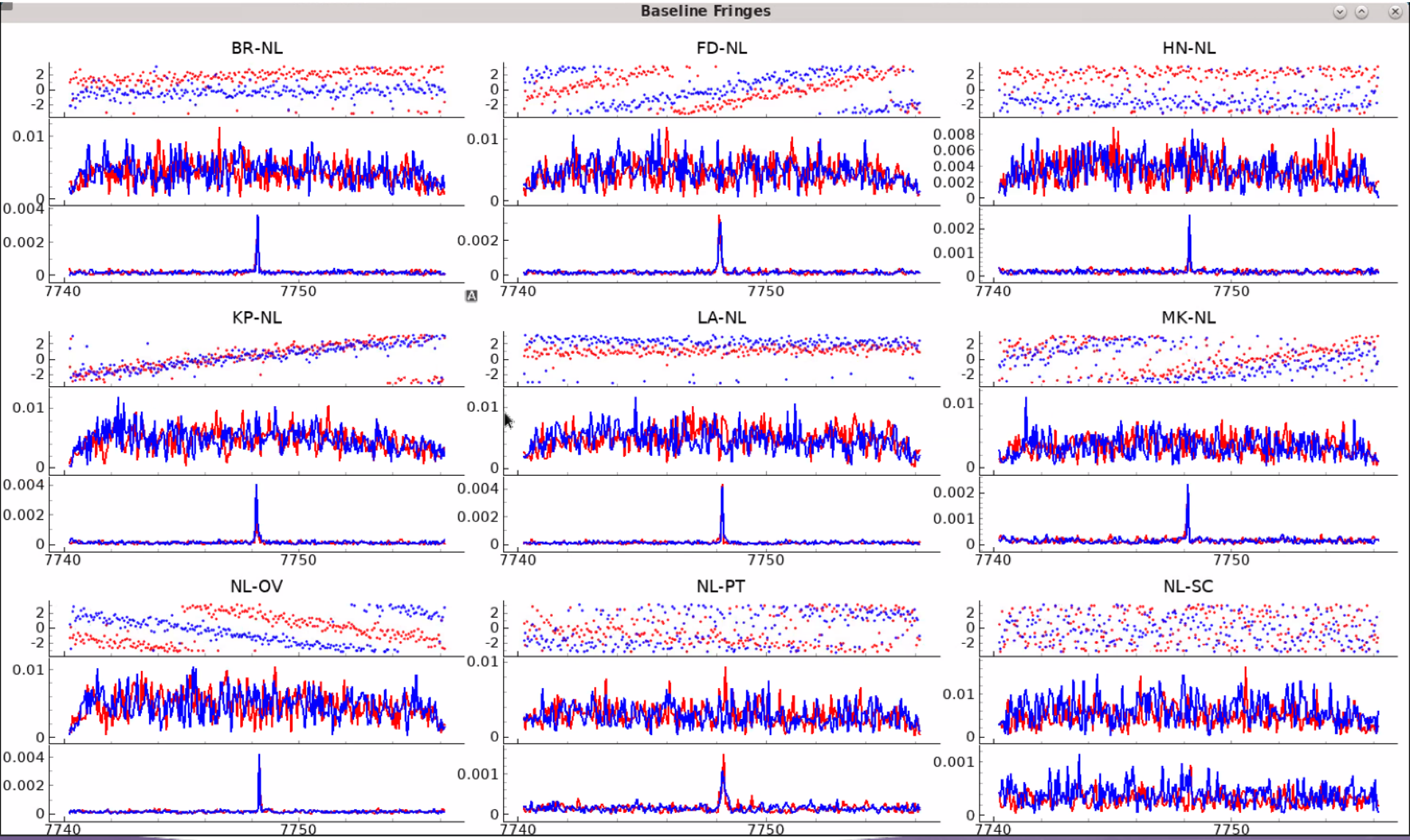
- Commercial Off-The-Shelf (COTS) hardware, firmware and software
- Let industry pay for most of the NRE
- Buy components with standard interfaces
- Upgrade in the future with expectation of compatibility
- Source from US supply chain to degree possible

- Some specific commercial offerings follow
  - VNDA not 100% tied to these solutions
  - Prototype is based on them

High speed networks to VLBA antennas

- NSF-funded effort
- Initial goals:
  - Establish minimum of 200 Mbps connectivity to each VLBA antenna
  - Deploy hardware at VLBA sites capable of eventual 10 Gbps speeds
  - *COMPLETE!*
- Stretch goals
  - Move recorder for one station to Socorro?
  - Invest in infrastructure for wider links?
  - Improve connectivity of VLBA operations center?
  - Better integrate near-real-time and real-time modes into VLBA operations model?

10-station real-time correlation at 128 Mbps



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Back-up slides for VNDA

VNDA Project Phases

- Phase 1: (Complete)
  - Risk reduction
  - Development of design concept
  - Conceptual design review
- Phase 2: (Oct 2020 to Dec 2021*)
  - Preliminary design
  - One VLBI baseband mode implemented
  - Zero baseline test
  - Preliminary design review

* *timelines are approximate*

VNDA Project Phases

- Phase 3: (Jan 2022 to Mar 2023*)
  - Final design
  - Deploy 2 units in field
  - Conduct fringe test
  - Final design review
- Phase 4: (Apr 2023 to Jun 2024*)
  - Procure and assemble production hardware
  - Install at all sites
  - Commissioning / science verification
  - Offer new capability to users

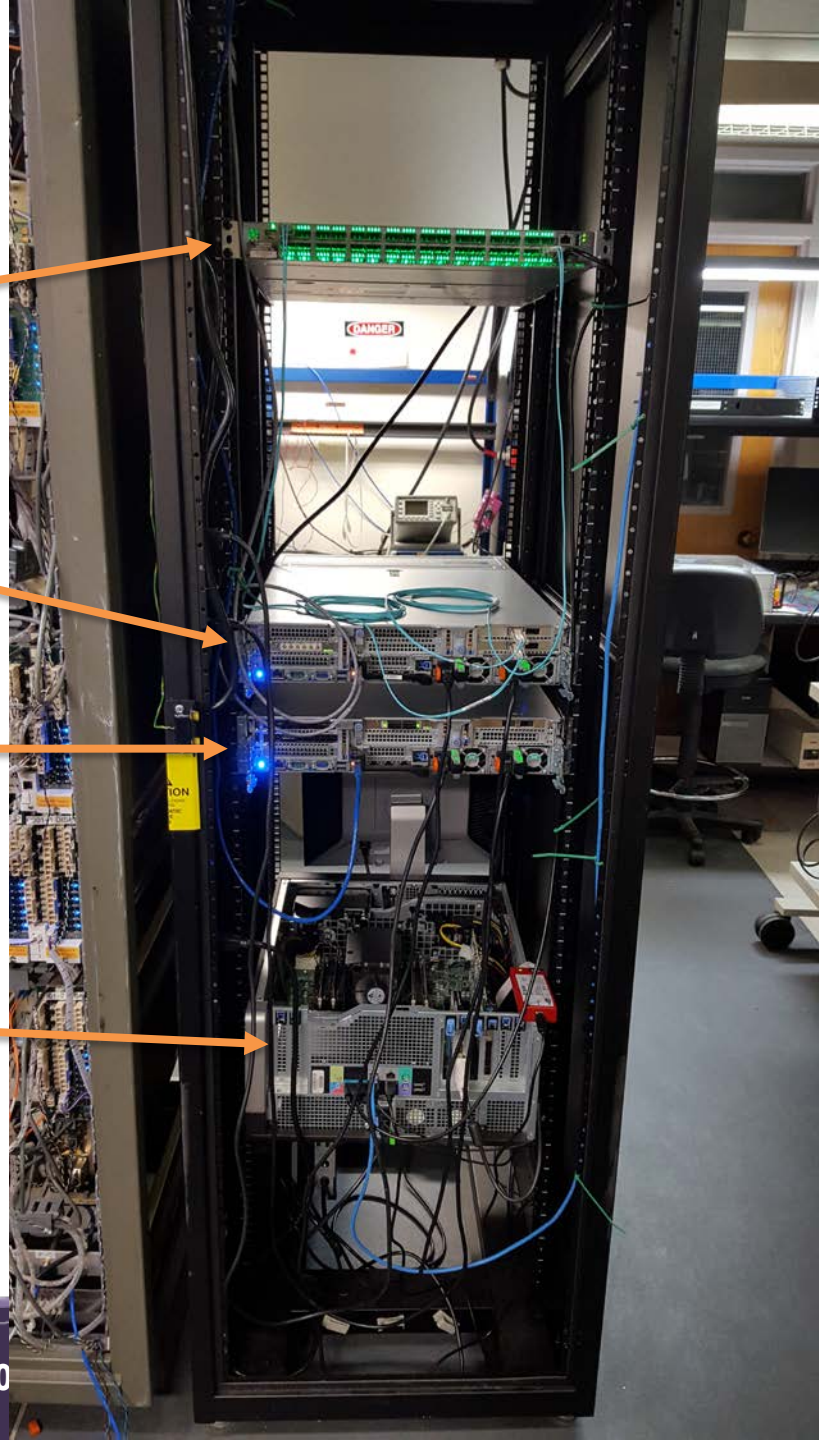
** attempts will be made to accelerate phases 3 and 4 by up to 9 months*

Major new components

- Sampler modules, in receiver cabin
  - Creates 4 "digital IFs", 1024 MHz bandwidth, in VDIF format
- 100 Gbps network switch
  - Fabric that connects all signal processing and recording components
- Channelizer module
  - Creates digital baseband channels
  - Requantizes to 2 (or other) bits per sample
  - Computes calibration metadata (switched power)
- Timing module
  - Need repeatable 1 PPS tick and clock signals in receiver cabin

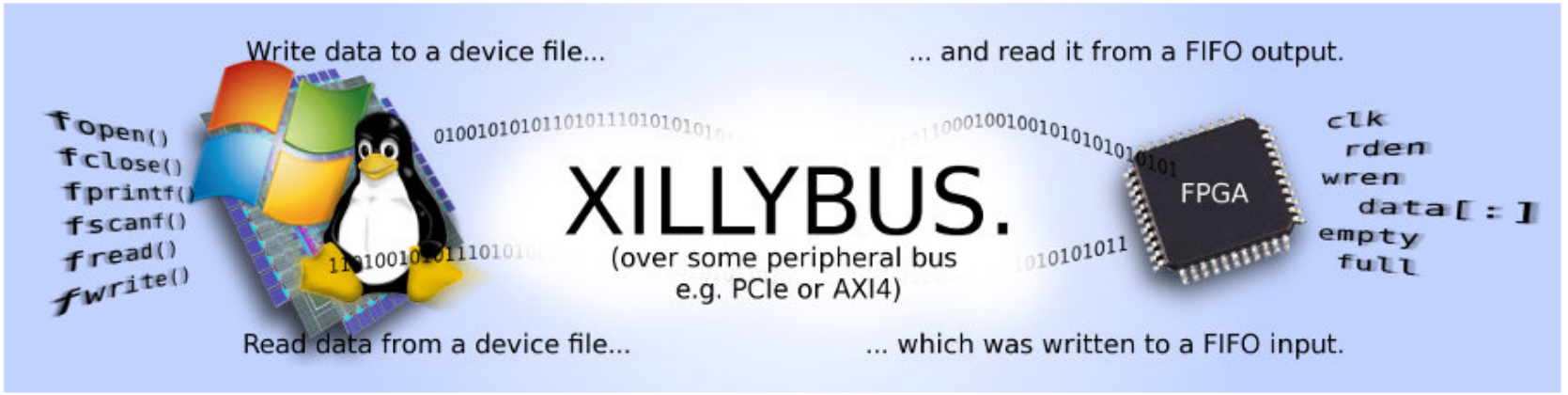
VNDA prototype rack

- 100 Gbps Switch
  - Fiber sources 8500-32c
  - 32 ports
- Sampler (Dell R740)
  - 2x dual 40Gb NICs
  - PCI592 w/ sampler module
- Channelizer (Dell R740)
  - PCI592 module
  - Also GPU
- Software dev system
  - With Xilinx evaluation kit



XILLYBUS. IP cores and design services

An FPGA IP core for easy DMA over PCIe with Windows and Linux



A simple turnkey solution

- Xillybus consists of an FPGA IP core and a driver for the computer: All the low-level design is already done. Read more...
- **Supported out of the box** by up-to-date Linux distributions.
- Drivers for Windows 7 and later available for download.
- FPGA designers interface with the IP core through a standard FIFO or dual-port memory
- Computer software programmers work in userspace with files, following classic UNIX

Features

- Very fast setup: A **day or two** is the typical lead time from downloading core & drivers to an end-to-end integration between host application and dedicated logic on FPGA.
- **Try it first**: Get your own **custom built IP core** for evaluation, and test it in your real design.
- **Portability**: Seamless transition between **Xilinx** and **Intel** FPGAs, **Linux** and **Windows**
- Robust pipe communication

Applications

- Data acquisition
- Video capture and playback
- Acceleration and HPC (High Performance Computing)
- FPGA control from host
- Easy design of peripherals
- Interface with dedicated hardware
- Logic verification on hardware
- Fast development of dedicated lab equipment
- Debugging
- Data interchange with High

Download

- IP core product brief

Download a working kit!

Try Xillybus with **your application data** from the FPGA to the host and vice versa. It's not just a demo, it works for real. Connect your application data to a standard FIFO, boot the computer or FPGA with

Xillybus

- Commercial solution to FPGA ← → CPU communication
- Modern Linux kernels have native support
- Maps data streams on FPGA to file streams in Linux
- Demonstrated on VNDA hardware at nearly full PCIe3 x8 speed
  - More than sufficient
- Supported by a wide array of PCIe FPGA hardware
- The company has been very supportive in initial development

PCI592 (similar products)

PCIe FPGA Carrier for FMC+, Kintex UltraScale™

- PCIe FPGA carrier for FMC+ per VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Active cooling for FPGA and FMC+
- Dual x8 lanes for direct connection to neighbouring FPGA card(s)

Download Datasheet Add to Info Request

PCI EXPRESS

The PCI592 is based on the Xilinx XCKU115 Kintex UltraScale FPGA, which provides 5,520 DSP slices, 75.9 Mb RAM and 1,451,000 logic cells. The FPGA interfaces directly to the FMC+ DP-23 and all FMC+ LA/HA/HB pairs, making it compatible with a wide range of industry standard VITA 57 modules. It also has interface to three DDR4 memory channels (2x 64-bit wide and 1x 32-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The unit has x8 PCIe edge connector routed to the FPGA PCIe Gen3 hard IP block. In addition, 16 uncommitted connection pairs are routed to a dual x8 expansion connector, providing direct connectivity to a neighbouring FPGA (e.g. via Aurora, 10G/40G, SRIO, PCIe) without the need to go through the host.

PCI592 provides active cooling of the FPGA and FMC+ (the module does not support HSPCe connector) making it appropriate for power-hungry applications or those requiring temperature stability for good performance.

CONTACT SALES TEAM

WHERE TO BUY

QUALITY ASSURANCE

Sampler module with standard FMC interface

FMC217

FMC ADC 12-bit @ 6.4 GSPS and DAC 16-bit @ 12 GSPS

Key Features

- ADC ADC12DJ3200
  - Option for ADC12DJ270
  - 8 JESD204B lanes from the ADC is routed to the FMC
  - 12-bit @ 6.4 GSPS
  - Wide full power bandwidth supports IF sampling of signals up to 6 GHz
- DAC AD9164/AD9162
  - 16-bit @ 12 GSPS
- FPGA Mezzanine Card (FMC) per VITA 57
- Excellent dynamic performance
- Front panel interface includes CLK In, Trig In and Trig Out

Benefits

- High dynamic range for versatility in video/broadcast requirements

Back-up slides for high speed networks

Detailed status by antenna site

- BR: connected at 200 Mbps
- FD: connected at 200 Mbps
- HN: connected at 2000+ Mbps
- KP: connected at 1000 Mbps
- LA: connected at 10,000 Mbps
- MK: connected at 1000 Mbps
  - Pursuing 10,000 Mbps option
- NL: connected at 200 Mbps
- OV: connected at 1000 Mbps
- PT: connected at 1000 Mbps
- SC: connected at 200 Mbps

Endpoint at VLBA operations center

- VLBA operated out of NRAO building in Socorro NM
  - Connected to outside world at 10 Gbps
- VLBA equipment rack connected to network by 3x 1 Gbps links
- These links will soon be the bottleneck for VLBA data transfer
- No firm plans to improve on this, but this could change

Associated efforts

- Software to make use of links is out of NSF project scope
  - Being supported out of VLBA operations funding
- Capability #1: near-real-time diagnostics
  - "Fringe test" capability in IOC
- Capability #2: real-time data transfer
  - Demonstrated from 8 antennas
  - In limited use for some tests
  - NRAO network supports cumulative data rate up to 3 Gbps
- Capability #3: real-time data processing (correlation)
  - Demonstrated; IOC expected by end of FY21
- Capability #4: full rate data recording (one station)
  - Will be investigating this option in coming year