Progress on EXPreS at JBO

Ralph Spencer

SA: eMERLIN out
Fabric: Protocols, Onsala-eMERLIN in

Personnel changes:

- Jan 08 Richard Hughes-Jones left to join DANTE (but Visiting Fellow at The University of Manchester)
- Jan 08 Simon Casey joined Onsala (gained PhD in Dec 2008)
- Stephen Kershaw left July 2008 (joined HorNet university Halls Of Residence Network, writing up for an MPhil)
- Tony Rushton will join EXPReS for a short period on submission of his PhD – subject to board approval??

E-MERLIN Out (SA)

- Progress with e-MERLIN (JH, STG):
  - Correlator racks arrived and powered up
  - Station board arrived – firmware being implemented
  - Correlator boards expected and remaining station boards expected ~April
  - Digital links being implemented on local telescopes

E-MERLIN progress

- Expect further station boards and one baseline board this week

- Expect full system by spring/early summer.
- Correlator passed CDR at NRAO – no further debuggung required

E-MERLIN Out (SA) contd

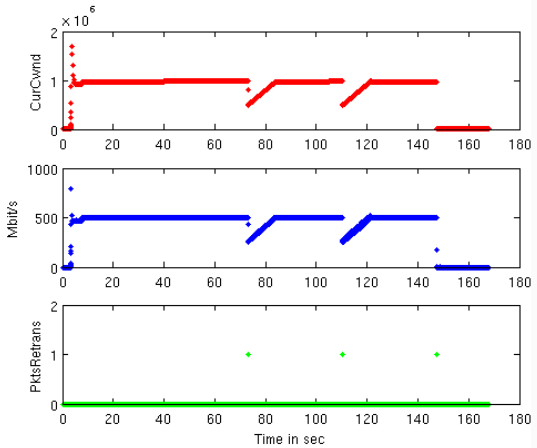
- Alternative multi-telescope connection to JIVE (PB)
  - Using existing analogue links and VLBI equipment
  - One wideband (<=1Gbps) Station (local telescopes)
  - One Outstation Terminal ('VLBA DAR')
  - Outstations use only 128mbps max
  - Therefore can add extra stations to VLBA DAR
  - Suitable for recording or fibre transmission
  - JIVE Correlator Network duplicates data stream
  - Some logistical/connection constraints, uses 2x1 Gbps external links

Haystack Recording Experiment

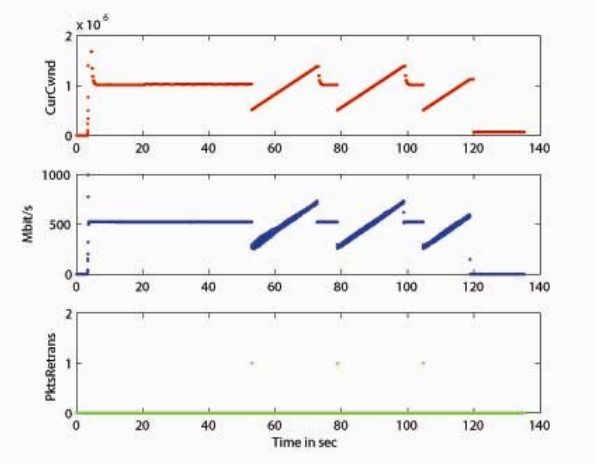
- Record entire Merlin set on one Mark5 Disk
- Use just one polarization, and above methods
- Four telescopes into VLBA system, one per IF
- Two telescopes into Local system, one per IF
- (only two IF ip's available on local system)
- Needed for multiple correlations with different field centres for wide field observations (Lonsdale, M31)

FABRIC: Protocols

- Final report on protocol performance nearly ready
- Written by Stephen Kershaw, being revised by RES and RHJ
- Need comments and a few words from Arpad re multi-tasking.



(a) 0.9 Mbyte (BDP) buffer

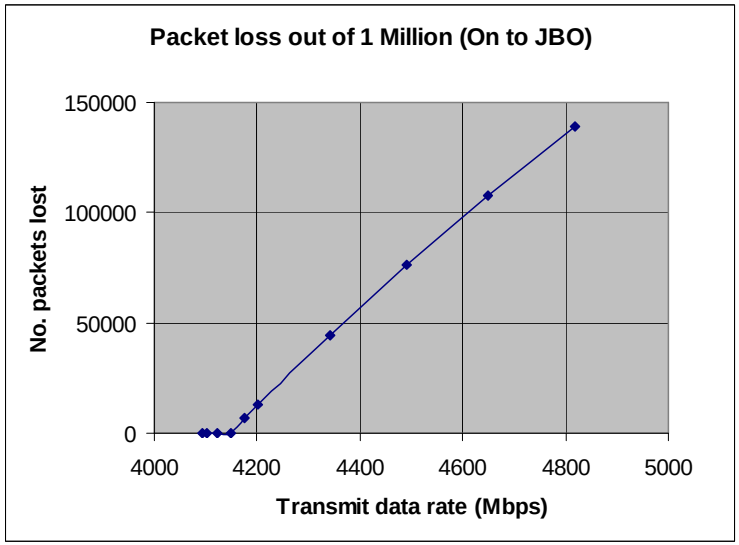


(b) 160 Mbyte (180x BDP) buffer

Progress Testing 10Gb Links ----(1)

eMERLIN IN: Onsala to Jodrell

- Tests in December 2008: link from Onsala to Jodrell is working well at up to 4.1Gbps
- There is no packet loss up to 4123Mbps
- Tests are continuing to characterise the link in both directions: transit times and 'bunching'.
- A 16 packet high speed buffer has been added to the receive iBOB design to reduce packet loss due to bunching



Packet loss for one million 8192 byte packets: iBOB at Onsala to iBOB atJBO

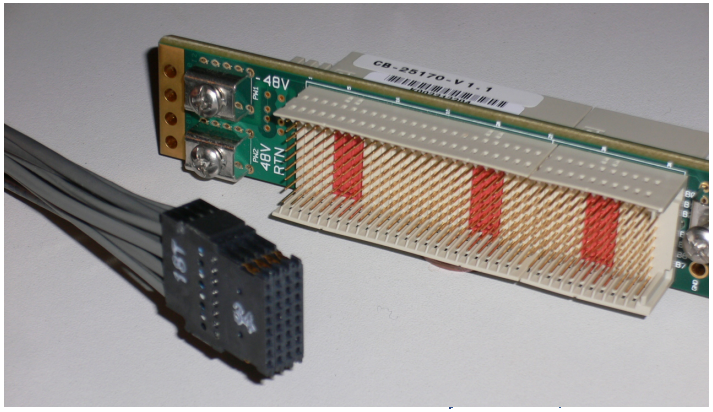
Progress Testing 10Gb Links ----(2)

eMERLIN OUT: Jodrell to JIVE

- Standardize on the proposed VDIF application header, preceded by a 63 bit packet sequence number
- Conversion to Mk V frames done in software at JIVE
- iBOB set up to store a test pattern or snapshot of data in SRAM and spool it out at 1Gbps; to be used to test the link from Jodrell to JIVE while the eMERLIN correlator is being commissioned

Progress integrating with eMERLIN

- The correlator backplane I/O standard is eight row 2mm hard metric (HM) connectors (Top photo shows the back of the SB rack)
- Meritec cables used, connecting to Meritec ‘wafers’, rather than ribbon cable as orginally planned on flexibility grounds
- Inputs and outputs from different station boards can now be mixed on one iBOB ZDOK connector, one iBOB can process the data from two station boards
- A PCB to interface the 2mm HM backplane connector to the ZDOK is currently being fabricated. A mounting plate has been designed to support the iBOB and converter boards in the rack



FPGA Firmware Development

- A Finite Impulse Response (FIR) filter has been designed to take a 64MHz, 8 bit, or 128MHz, 4 bit signal from a filter chip and produce 8 or 16 VLBI compatible output bands. Simulation indicates that the filter will fit in the VSI chip, along with code to remove the eMerlin delay and station frequency offset

- A test configuration for the VSI chip has been coded in VHDL. One of the 18 filter bank chip outputs can be selected. Data from this chip are assembled into 32 bit words and sent to an iBOB. The iBOB will capture a snapshot of data from one or both polarizations in SRAM, which can be used to verify operation of the station board

- Graphical interface panels for the VSI chip configurations (export, import, and test) have been derived from the existing station board GUI java code. These may be used to select data source, frequency band etc., and monitor the data flowing through the VSI chip

Conclusion

- Good progress in implementing hardware and software, with most deliverables met
- Good prospect of astronomical tests at 4 Gbps between Onsala and JBO before end of August - depends on delivery of a correlator board
- Need the 4.1 Gbps link until at least then.