Correlator meeting, Arpad's room, September 13 2012, 11.00 am
Present: Jintao, Salvatore, Jonathan, Des, Harro, Arpad

agenda

actions:

Jonathan: test fix of Erlang performance problems reading UDP packets (on hold)

Jonathan + Salvatore: figure out how to make packet spacing adjustable (on hold)

Des + Harro: come up with list of the parts of software that are done, need work, need writing, and an indication of time involved
#done remove

Jintao: write down his questions on pulsar gating and then talk about it with Aard
#done remove

Harro: write up a small doc about timing mechanism
#not done,remains

topics:

new FFT
delay correction
pulsar gating
timing of correlator
actual tests
timeline

aob

next meeting

-new FFT

Jonathan: keep freq at 266MHz. Two data streams in parallel. Filter bank changed, ready for synthesis and simulation. Synthesizing complete FN design, see if it fits. New FFT seems less time critical, which is good. Changes to packet RX by Jonathan needed. Simulation next week? Also change in phase delay module. Tomorrow?

-delay

Jonathan: in principle all is there, need to get data in and out, all 4 FNs at same time.

-pulsar gating

Jintao: packet format to be decided, transfer of coefficients, distinction between delay/pulsar coefficients. Jonathan: after off-load port the choice is made between phase and delay, should also be capable of distinguishing pulsar coeffiecients.
Jintao is thinking of using either on-board memory or DDR. Long latency (30 to 50 clock cycles) for DDR, need to store in FIFO in advance.

Long discussion about number of waveforms, where to generate them, where to send them (FN or BN), how to synchronise them with data, send them via NIOS or via 10G ports.

Size seems to be fixed to 1kbit per waveform, depending on size of FFT (which is fixed for the time being). Need 16 waveforms, but maybe more for high dispersion pulsars, which means DDR memory is needed. Jintao thinks the waveforms should be generated on control computer, need to load 4Mbits of waveforms once per scan/pulsar.

If NIOS is to be used with DDR, need DDR controller, maybe better use UDF offload port.
Maybe calculate waveforms in real time on control computer, send them to FN, no need for DDR. Des thinks it will be too much data. Maybe not quite in real time, send blocks to FIFO. Jonathan suggests to send one waveform + offsets.

Probably best via 10G. Here we find out that gating is to be applied before accumulation on BN. Could be sent to 10G on BN (although now unidirectional), could be applied after correlation but presumably not enough resources on BN, and synchronisation basically impossible.

Use FN anyway, apply gating after filterbank, before hitting the mesh. Use same synchronisation method as with delay coefficients, either square matrix stored or streaming. Latter is more flexible, preferable.

Jintao to write this up in his design doc!! ****Action

After lunch, continuation with only Salvatore, Harro, Des, Arpad

Harro brings up a potential problem with new synch mechanism. Data is read into memory but FFT blocks might straddly 1 second blocks. Need integral number of FFTs per sec, this we probably can guarantee. Talk about limiting bandwidths to powers of 2, also integration times. Lengthy discussion, finally agreed upon method that will allow any integration time, divide memory into 4 blocks, alway one block between the one that is being read and being written, enough memory for 4 bits data, 8GB memory modules will be used if we ever go to more than 4 bits. Slight change to synch mechanism, but nothing dramatic.

Harro to write this up, already action

next meeting: next Thursday