

Correlator Implementation and Control meeting

Thursday March 11, 2010, Muller room

Present: Jonathan, Ying, Eric, Raj, Harro, Des, Sergei, Paul, Arpad

Agenda

- test firmware, status and timeline
 - correlator firmware
 - correlator control code and NIOS OS
- test firmware

Jonathan: 10G connections: need limited functionality:: UDP, ping, ARP, do all of it in hardware. For UDP: re-use Casper firmware. Implementing interface between 10G and state machine

Other side of chip: block of 16 transceivers. Mapping is different for every FPGA (8 possible mappings, layout driven). Timing is still a problem at double data rate. Frame (dis)assembly will be done by VHDL state machine

Harro: maybe simplification possible, by bypassing NIOS processing for handling packets. Not clear if this is worthwhile, because of use of extra logic

Eric: using modelsim on PC to communicate w 1G ethernet. Use of Tkl scripts to generate packets. Should be done in couple of weeks. Daniel is testing transceivers, made small application for send/receive, with LEDs. Mesh nearly finished, one more week needed. Will also be useful on 10G ports.

Plan is to develop test images, and from that an integrated test env, which will be the platform on which applications are built. The applications will be able to function with or without the test functionality. Hopefully, end of April this will all be done.

- correlator

still too early, only bits and pieces of test firware which will be used in application

Raj: FFT finished with automatic scaling (optimal SNR). input 10 bits -> 17 bits through bit growth. Optimum performance within certain parameters. EVN 75 case dB, Apertif 72 dB. Limited to 275 MHz, probably because of buffering problems. Purely home written: comparisons with "standard" windowing fie needed. Tweaking needed for higher speed, optimisation of use of resources. Raj will has written and will distribute document.

- control code

Harro: after review of Jonathans design document, change of implemtation, plus changes in NIOS code

Des: VDIF data generator (nearly) done, data comparison on software correlator. Exact comparison difficult because of header replacement, but convincing enough. Sergei explains replacement should be zeros. Des will tell Aard. Now working on Erlang VEX parser/mySQL database. About one month work, then should talk with support scientists.

next meeting: about one month from now